

AMENDMENTS TO THE CLAIMS

1. (Original) A monolithic semiconductor device comprising:

a semiconductor substrate;

a plurality of upright free-standing microstructures formed over the substrate; and

a brace transversely extending between lateral sides of at least two of the free-standing microstructures.
2. (Original) The semiconductor device according to claim 1, wherein the brace interconnects substantially all of the microstructures.
3. (Original) The semiconductor device according to claim 1, where the brace is located substantially near upper ends of the microstructures.
4. (Original) The semiconductor device according to claim 1, wherein the brace has a width approximately equal to or less than the largest cross-sectional dimension of the microstructures.
5. (Original) The semiconductor device according to claim 1, wherein the brace comprises a microbridge structure extending above the substrate and between two or more of the microstructures.
6. (Original) The semiconductor device according to claim 1, where the microstructures each comprise a conductor material portion

standing upright over the substrate, and wherein the brace interconnects the conductor material portions of two or more of the microstructures.

7. (Original) The semiconductor device according to claim 1, wherein the microstructures comprise generally cylindrical container shapes and the brace comprises a microbridge structure.

8. (Original) The semiconductor device according to claim 1, wherein the microstructures comprise generally solid cylindrical shapes and the brace comprises a microbridge structure.

9. (Original) The semiconductor device according to claim 1, where the brace comprises a dielectric material.

10. (Original) The semiconductor device according to claim 1, further comprising a dielectric layer between the substrate and the brace, where the brace is vertically spaced from the dielectric layer.

11. (Original) The semiconductor device according to claim 1, wherein the microstructures comprise conductive material and the brace comprises a dielectric.

12. (Original) The semiconductor device according to claim 1, wherein the microstructures are defined within an active circuit area, and further comprising a die having non-active circuit areas located adjacent the active circuit area, wherein the brace further interconnects at least two of the microstructures with non-active areas of the die.

13. (Original) The semiconductor device according to claim 1, wherein the microstructures are stud capacitors.

14. (Original) The semiconductor device according to claim 1, wherein the microstructures are container capacitors.

15. (Original) The semiconductor device according to claim 1, wherein the microstructures comprise double-sided container capacitors.

16. through 22. (Cancelled)

23. (Previously Presented) A semiconductor storage capacitor, comprising:

a semiconductor substrate;

a plurality of upright free-standing capacitor storage node microstructures formed over the substrate; and

a brace transversely extending between lateral sides of at least two of the free-standing microstructures, wherein the microstructures comprise generally solid cylindrical shapes and the brace comprises a microbridge structure.

24. through 27. (Cancelled)

28. (Previously Presented) A semiconductor storage capacitor, comprising:

a semiconductor substrate;

a plurality of upright free-standing capacitor storage node microstructures formed over the substrate; and

a brace transversely extending between lateral sides of at least two of the free-standing microstructures, wherein the microstructures comprise stud capacitors.

29. through 38. (Cancelled)

39. (Previously Presented) A memory circuit, comprising:

a semiconductor substrate having a memory cell including diffusion regions;

a dielectric layer on the substrate;

conductive plugs extending vertically from an upper surface of the dielectric layer to respective diffusion regions;

a plurality of upright free-standing capacitor storage node microstructures each formed over the dielectric layer and a respective conductive plug; and

a brace transversely extending between and laterally supporting respective lateral sides of at least two of the free-standing microstructures, wherein the microstructures comprise generally solid cylindrical shapes and the brace comprises a microbridge structure.

40. through 43. (Cancelled)

44. (Previously Presented) A memory circuit, comprising:

a semiconductor substrate having a memory cell including diffusion regions;

a dielectric layer on the substrate;

conductive plugs extending vertically from an upper surface of the dielectric layer to respective diffusion regions;

a plurality of upright free-standing capacitor storage node microstructures each formed over the dielectric layer and a respective conductive plug; and

a brace transversely extending between and laterally supporting respective lateral sides of at least two of the free-standing microstructures, wherein the microstructures comprise stud capacitors.

45. and 76. (Cancelled)

77. (Previously Presented) A processor system, comprising:

a processor; and

a memory circuit fabricated on a semiconductor chip communicating with the processor, said memory circuit comprising:

a semiconductor substrate having a memory cell including diffusion regions;

a dielectric layer on the substrate;

conductive plugs extending vertically from an upper surface of the dielectric layer to respective diffusion regions;

a plurality of upright free-standing capacitor storage node microstructures each formed over the dielectric layer and a respective conductive plug; and

a brace transversely extending between and laterally supporting respective lateral sides of at least two of the free-standing microstructures, wherein the capacitor microstructures comprise capacitor studs.

78. (New) A support structure on a semiconductor device comprising:

a plurality of braces transversely extending between lateral sides of a plurality of microstructures formed over a semiconductor substrate, wherein said plurality of braces comprise a support structure for said plurality of microstructures.

79. (New) A brace for a semiconductor device comprising:

at least one brace transversely extending between lateral sides of at least two of a plurality of microstructures on a semiconductor substrate, wherein said at least two of said plurality of microstructures are supported only by said at least one brace.

80. (New) An in-process semiconductor device comprising:

a semiconductor substrate;

a plurality of microstructures formed over the substrate; and

at least one brace transversely extending between lateral sides of at least two of said plurality of microstructures, wherein said at least two of said plurality of microstructures are supported only by said at least one brace.

81. (New) A semiconductor support structure, comprising:

a semiconductor substrate;

a plurality of microstructures formed over the substrate; and

at least one brace transversely extending between lateral sides of at least two of the microstructures, wherein the brace comprises a support structure.

82. (New) The semiconductor support structure of claim 81, wherein said at least one brace comprises a plurality of braces.

83. (New) The semiconductor support structure of claim 82, wherein said plurality of braces form a lattice support structure.

84. (New) A semiconductor storage capacitor, comprising:

a semiconductor substrate;

a plurality of capacitor storage node microstructures formed over the substrate, said microstructures having vertical surfaces;

a brace transversely extending between the vertical surfaces of at least two of the microstructures, said brace being located substantially near the upper ends of said vertical surfaces of said microstructures; and

a vertical space between said brace and said substrate.

85. (New) A semiconductor storage capacitor, comprising:

a semiconductor substrate;

a plurality of capacitor storage node microstructures formed over the substrate, said microstructures having vertical surfaces; and

a plurality of braces transversely extending between the vertical surfaces of at least two of the microstructures, said brace being located substantially near the upper ends of said vertical surfaces of said microstructures.